

**Notic of Allowability**

Application No.

10/023,819

Examiner

John B. Vigushin

Applicant(s)

CHANDRAN ET AL.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to RCE filed 19 March 2004.
2. ☒ The allowed claim(s) is/are 1-29.
3. ☒ The drawings filed on 21 December 2001 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Not the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 0304
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_.

John B. Vigushin  
Primary Examiner  
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### DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on March 19, 2004 has been entered.

### ***Allowable Subject Matter***

2. Claims 1-29 have been allowed.
3. The following is an examiner's statement of reasons for allowance:

As to Claims 1-9, patentability resides in *thermally expanding each of the semiconductor chip and substrate substantially the same amount in a direction along surfaces thereof to be joined by soldering*, in combination with the other limitations of base Claim 1.

As to Claims 10-13, patentability resides in *thermally expanding each of the first and second members substantially the same amount in a direction along surfaces thereof to be joined*, in combination with the other limitations of base Claim 10.

As to Claims 14-16, 20, 21 and 22-24, 28, 29, patentability resides in the limitation wherein *the magnitude of the elongation mismatches and the stresses induced thereby in the electronic assembly are less than one-half that expected based*

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*upon cooling the substrate and semiconductor chip from the solder solidification temperature to room temperature following soldering of the soldered joints*, in combination with the other limitations of base Claims 14 and 22, respectively.

As to Claims 17-19 and 25-27, patentability resides in the limitation wherein *the soldered joints connect the semiconductor chip to the tops of respective ones of the standoff elements*, in combination with the other limitations of base Claims 17 and 25, respectively. Although Farnworth et al. (US 6,002,590) in Fig. 9 and Iijima et al. (US 2001/0008309 A1) in Figs. 3, 4 and 5A,B disclose *soldered joints connecting the semiconductor chip to the tops of respective ones of the standoff elements* in order to relieve the stress on the solder joints (composition and melting point unspecified in Farnworth et al. and Iijima et al.) due to thermal coefficient mismatch between the chip and the substrate, and Research Disclosure (RD 291011) discloses a chip with high melting point solder bump D mounted to the tops of standoffs ABA' on substrate H, where A and A' are low temperature solder and B is high temperature solder, and the standoffs ABA' enhance the height of the chip pad sites of the substrate, thereby relieving stress on the solder joints due to thermal coefficient mismatch between chip and substrate, nevertheless Farnworth et al., Iijima et al. and RD 291011 do not alone or in any combination suggest combining the stress-relief standoff elements as a supplemental stress-relief structure to function in conjunction with the stress-relief annular ring of Dauksher et al., neither Dauksher et al. nor Farnworth, Iijima and RD 291011 suggesting how, or whether, standoff elements could positively improve or affect the stress-relief already provided by the annular ring of Dauksher et al.

Furthermore, modified Dauksher et al. (US 6,320,754 B1; see rejections of originally filed Claims 14 and 22 in the Office Action of May 06, 2003) discloses all the limitations of the claims including the resultant shear and stress on the solder joints with and without the annular ring 506 designed to reduce the CTE induced elongation mismatches at a specified temperature (col.3: 41-43). However, modified Dauksher et al. does not teach or fairly suggest any additional supplemental combination with the specific standoff structures of Farnworth et al., Iijima et al. or RD 291011, or provide any positive indication how such a combination would affect, supplement or substantially improve the desired stress-relief result already achieved solely by the annular ring 506 of Dauksher et al. (*Examiner's Note*: Dauksher et al., Iijima et al. and RD 291011 are already of record in the instant RCE Application).

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Claims 1-16, 20, 21, 17-19, 22-24, 28, 29 and 25-27 of the instant allowed Application will be renumbered as Claims 1-29, respectively, for publication in the issued patent.

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Farnworth et al. (US 6,002,590) discloses soldered joints connecting the semiconductor chip to the tops of respective ones of standoff elements in order to relieve the stress on the solder joints (see discussion under the reasons for allowance of base Claims 17 and 25, in section 3, above).

Jimarez et al. (US 6,664,637 B2; Figs. 7-8), Sarkhel (US 6,581,821 B2; Fig. 1), Schreiber et al. (US 5,790,377; see Figure) and Love et al. (US 5,773,889; Fig. 4) all disclose soldered joints connecting the semiconductor chip to the tops of respective ones of standoff elements in order to relieve the stress on the solder joints.

Ozoe (JP09-275107 A; *already made of record in the instant RCE Application*) discloses forming bumps on a wafer using a transfer board, wherein the transfer board 3 and wafer 1 are heated at different temperatures so that the their thermal expansion is the same to ensure optimal transfer of solder 4 from transfer board 3 to the copper bump pads 2 of wafer 1. Ozoe does not teach mounting a finished, bumped wafer to a circuit substrate using the above-disclosed technique equal thermal expansion of elements.

Del Monte (US 4,481,403; *already of made of record in the instant RCE Application*) discloses a temperature control circuit distributed between a chip and substrate device such that during the operational temperature cycles of the device, the circuit controls the heating of the chip and the substrate so that the chip and substrate thermally expand and contract at the same rate, thereby reducing or eliminating stress on the solder joint connections 14 and 16 (Fig. 1; col.1: 44-col.2: 6). Del Monte teaches this control circuit for the operation of an already-assembled chip and substrate device

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and neither teaches nor fairly suggests its use in the fabrication of the device; i.e., does not teach or fairly suggest mounting the chip to the substrate using such a temperature control circuitry to control the fabrication temperatures required to solder the chip to the substrate in such a manner that the chip and substrate have the same thermal expansion for eliminating thermal stresses on the solder joints during the chip mounting process.

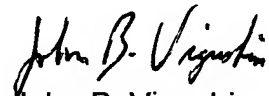
Zhang et al. (US 6,310,403 B1; Figs. 1-3) and Marion et al. (US 6,170,155 B1; Figs. 4-6) [*both Zhang et al. and Marion et al. already made of record in the instant RCE Application*] teach pad pitch compensation of the thermal expansion mismatch between chip and board in order to relieve the stress on the solder joints after the chip has been mounted to the substrate. Zhang et al. and Marion et al. do not teach or suggest a means for matching the thermal expansion of chip and board for achieving solder joint stress relief.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin  
Primary Examiner  
Art Unit 2827

jbv  
May 31, 2004